Name:.....
Roll No:.....

MAR ATHANASIUS COLLEGE OF ENGINEERING
KOTHAMANGALAM – 686666
(Govt. Aided Autonomous Institution)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.TECH SECOND SERIES EXAMINATION, OCTOBER 2026

(S5 ECE A & B) B24EC3T04 - VLSI DESIGN

Max. Marks: 40 Duration: 1.5 Hours

PART A

Answer all questions. Each question carries ***3 marks.***

1. While using an NMOS transistor as a pass-transistor switch to transmit a HIGH signal, the output never reaches full V_{DD}. Justify why the NMOS transistor can pass only a 'weak logic 1'. (CO3)

2. As a chip design intern, before creating the actual mask layout of a CMOS inverter, plan the placement of different layers using a simplified representation. Construct the stick diagram of the gate, clearly indicating the different layers. (CO3)

3. An engineer is designing a digital logic circuit using complementary CMOS technology. Determine the number of NMOS and PMOS transistors required for the implementation of the Boolean function:

$$Y = \overline{ABD + C}$$ (CO3)

4. A 16-bit ripple carry adder is implemented using multiple full adders. For each full adder, the propagation delay for the sum is 4 ns and the propagation delay for the carry-out is 3 ns. Calculate the total propagation delay for the ripple carry adder. (CO4)

PART B

Answer all questions. Each question carries 14 marks.

5. a) A CMOS inverter is used in a digital circuit to convert an input logic signal into its complementary output. Explain the DC characteristics of the CMOS inverter with the help of suitable diagrams. (7 marks, CO3)

5. b) As a VLSI layout engineer, you need to translate the schematic of a 2-input NAND gate into its actual mask layout for fabrication. Draw the physical layout of the gate using λ-based design rules and mark the relevant width, spacing, and overlap requirements. (7 marks, CO3)

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6. a) You are tasked with designing a full adder for a low-power arithmetic unit, where full-swing output is essential. Realize the full adder using Transmission Gate logic, mentioning all the design steps involved. (7 marks, CO3)

6. b) You are designing a fast n-bit adder for a processor's ALU where carry propagation delay must be minimized. Explain the concept of a Carry Bypass Adder and analyze how it reduces this delay. Illustrate the operation using a suitable block diagram. (7 marks, CO4)