Name:.....

Roll No:.....

MAR ATHANASIUS COLLEGE OF ENGINEERING
KOTHAMANGALAM – 686666
(Govt. Aided Autonomous Institution)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B. TECH SECOND SERIES EXAMINATION, OCTOBER 2026

(S5 ECE A & B) B24EC3P14 :DIGITAL SYSTEM DESIGN

Max. Marks: 40 Duration: 1.5 Hours

PART A
Answer all questions. Each question carries 3 marks.

1.	A circuit produces a momentary logic 1 when the output should remain at logic 0 during a change in one input. Identify the hazard and explain how it can be eliminated.	(CO3)
2.	In an FPGA-based system, the clock reaches two different regions of the chip at different times. Explain the difference between clock skew and clock jitter and state one practical method to reduce each.	(CO3)
3.	Explain the Design steps for a fault cover table method.	(CO4)
4.	Explain the types of hazards with suitable examples.	(CO4)

PART B
Answer all questions. Each question carries 14 marks.

5.	a.	A static zero hazard is present in the given circuit, **Y = X1.X2 + X2'.X3** Obtain the hazard free circuit .	(CO3) (7 marks)

P.T.O.

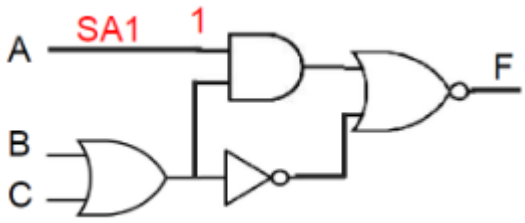
VISION
Embedding Creativity and fostering quality Education
MISSION
Advance the field of Electronics and Communication by developing and disseminating innovative practices and technologies.

Nurture technically competent professionals in Electronics and Communication Engineering equipped with the skills to address global challenges.

Foster socially responsible technocrats and entrepreneurs who contribute positively to society through their expertise and leadership.

b. Differentiate between static 0 and static 1 hazard using suitable examples. (CO3) (7 marks)

6 a. Find the Test Vectors for the given circuit using Boolean Difference method (CO4) (7 marks)



b. Find the test vector of all SA0 and SA1 faults of the circuit whose Boolean function f =x1 x2 + x1 x3'x4' + x2 x4 by the Kohavi algorithm. (CO4) (7 marks)

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