MAR ATHANASIUS COLLEGE OF ENGINEERING, KOTHAMANGALAM

(GOVERNMENT AIDED AUTONOMOUS ENGINEERING COLLEGE)

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Second Sessional Examination October 2026

B24EE2T03 DIGITAL ELECTRONICS

(S3_EA & EB)

Max. Marks: 40 Time: 1 Hours 30 Minutes

Answer all questions from Part A and Part B

PART A (4X3=12 Marks)

1. Design an even parity generator. (CO3)
2. Develop a Full Adder circuit from its truth table and implement the circuit using logic gates. (CO3)
3. Implement a 2-bit ripple counter using D flipflop. (CO4)
4. Derive the excitation table of JK flipflop and draw its transition diagram. (CO4)

PART B (2X14=28 marks)

5. **a.** A smart parking system uses four sensors A, B, C, and D to monitor the status of four parking zones. The system should turn ON the parking warning indicator for the following sensor conditions: F=1 for sensor combinations corresponding to decimal states 0, 2, 3, 5, 7, 10, 12, and 15. For all other combinations, the warning indicator remains OFF. Design and implement the logic function using an 8:1 multiplexer.

   b. Design a digital circuit to check the equality of two 3-bit binary numbers. If the two 3-bit numbers are equal, the seven-segment display should display P, else the display should show F. Use a common-anode seven-segment display.

   (5 + 9 = 14 Marks) (CO3)

6. **a.** A digital system is provided with a 2 kHz square-wave clock signal. Design a digital circuit to obtain a clock signal of 125 Hz. Draw the circuit and explain the frequency division at each stage. Modify the same circuit to design a MOD-11 asynchronous counter.

(P.T.O.)

VISION

Endeavour to Ensure Excellence

MISSION

Mould technically competent and morally strong Engineers

Achieve dynamic leadership through quality Education

Cater the needs of industry and community through Emulation

Empower the students to serve the nation with Dedication