Name:.....
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MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS), KOTHAMANGALAM - 686666

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

B.TECH SECOND SERIES EXAMINATION, OCTOBER 2026 (S3 CS, DSA, DSB, AIML)

B24CS2T02 COMPUTER ORGANIZATION AND ARCHITECTURE

Max. Marks: 40 Duration: 1.5 Hours

PART A

Answer all questions. Each question carries 3 marks.

1. **What** are interupts, List the sequence of steps following an interupt request? **(CO3)**

2. **How** does scratchpad memory overcome the time complexity of accessing data in tight loops? **(CO4)**

3. **Explain** how a DMA controller transfers data between memory and an I/O device. **(CO3)**

4. **What** is the basic building block used in designing an arithmetic unit? **(CO3)**

PART B

Answer all questions. Each question carries 14 marks.

5. (a) **U**sing 4:1 multiplexers with two selection lines H1 and H0, synthesize a 4-bit shifter that implements Shl, Shr, Pass-through, Zero-fill. **Illustrate** and explain the gate-level diagram. **(CO4)**(7 marks)

   (b) **Design** an arithmetic circuit with one selection variable S and two data inputs A and B.When S=0,the circuit performs the addition operation F=A+B, when S=1 the circuit perform increment operation F=A+1. **(CO3)**(7 marks)

VISION

To mould competent computing professionals, innovators, and leaders guided by ethical values and committed to technological advancement and sustainable societal development.

MISSION

- Provide quality education through strong theoretical foundations, experiential learning, and exposure to emerging computing technologies.
- Cultivate critical thinking, research aptitude, and innovation through problem-based learning, industry interaction, and research initiatives.
- Foster ethical values, leadership, social responsibility, and an aspiration for lifelong learning through professional practices, teamwork, and mentoring.

6. (a) **C**onsider an 8-bank memory system. Each bank contains 32 data words, and each data word is identified by a word address. A program accesses the following word addresses: 0, 4, 8, 12, 16, 20, 24, 28.

(i) **Determine** the bank mapping for each address in both low-order and high order interleaving.

(ii) Will all memory accesses proceed in parallel? **Justify** your answer. **(CO5)**(6 marks)

(b) A file server uses a cache with 4 slots to store frequently accessed files, implementing the LFU replacement policy with a tiebreaker that evicts the least recently used file among those with the same frequency. The file request sequence is: FileA, FileB, FileA, FileC, FileB, FileD, FileA, FileC, FileE. The cache starts empty. Track the cache state determine hits, misses, and evictions for each request. **Calculate** the hit ratio. If the frequency are the same, FIFO (First-In-First-Out) is used as the final tie-breaker. Then, assess whether LFU is effective for this file server by comparing it with MRU.

(CO5)(8 marks)