Name:.....
Roll No:.....

MAR ATHANASIUS COLLEGE OF ENGINEERING
KOTHAMANGALAM – 686666
(Govt. Aided Autonomous Institution)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.TECH FIRST SERIES EXAMINATION, AUGUST 2026

(S5 ECE A & B) B24EC3T04 - VLSI DESIGN

Max. Marks: 40 Duration: 1.5 Hours

PART A

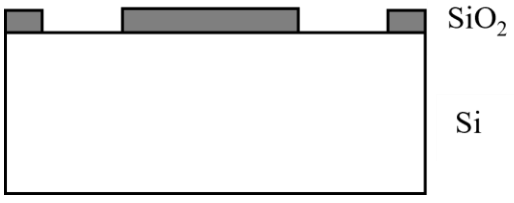
Answer all questions. Each question carries 3 marks.

1. Differentiate between dry etching and wet etching used for IC fabrication. (CO1)
2. A semiconductor fabrication company is manufacturing an integrated circuit containing MOSFETs. The gate oxide must be grown to a thickness of 0.15 μm on a freshly cleaned silicon wafer using dry oxidation at 1200°C. For dry oxidation at 1200°C, the Deal-Grove parameters are: B = 0.045 μm^2/hr, B/A = 1.120 μm/hr, and τ=0.027 hours. Determine the oxidation time required to achieve the specified oxide thickness. (CO1)
3. Differentiate between diffusion and ion implantation in the VLSI technology. (CO1)
4. A consumer electronics company has decided to use an ASIC instead of a general-purpose processor in its new smartwatch. Mention any three features of an ASIC that might have influenced the company's decision. (CO2)

PART B

Answer all questions. Each question carries 14 marks.

5. a) An aerospace sensor manufacturing company is developing a pressure sensor for monitoring cabin pressure in an aircraft. As a process engineer, you have been assigned the task of fabricating the SiO_2 layer on a silicon wafer according to the pattern shown below. The fabrication process must use positive photoresist and standard photolithography techniques. Describe the complete fabrication procedure, explaining each intermediate step with suitable diagrams. (7 marks, CO1)



5. b) A semiconductor manufacturing company is producing single-crystal silicon wafers for fabricating integrated circuits. As a process engineer, explain the Czochralski crystal growth process used to produce the silicon ingot. Illustrate the process with neat diagrams. (7 marks, CO1)

6. a) A space research organization is developing an onboard satellite communication system using an FPGA because of its flexibility for design updates. Explain the internal architecture of an FPGA with the help of neat diagrams and describe the role of each architectural block. (7 marks, CO2)

6. b) As a VLSI design engineer, explain the different types of ASICs with the help of neat diagrams, and mention the advantages/disadvantages of each type. (7 marks, CO2)