Name:.....
Roll No:.....

MAR ATHANASIUS COLLEGE OF ENGINEERING
KOTHAMANGALAM – 686666
(Govt. Aided Autonomous Institution)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B. TECH FIRST SERIES EXAMINATION, AUGUST 2026

(S5 ECE A & B) B24EC3P14 DIGITAL SYSTEM DESIGN

Max. Marks: 40 Duration: 1.5 Hours

PART A

Answer all questions. Each question carries 3 marks.

1. Sketch the Moore and Mealy model state diagrams for sequence detector. (CO1)

2. Draw the ASM chart for a mod-3 up counter. (CO1)

3. Discuss synchronous and asynchronous sequential circuits with block diagram. (CO2)

4. List the steps involved in synchronous sequential circuit analysis. (CO2)

PART B

Answer all questions. Each question carries 14 marks.

5. a. Minimize the given table using Implication chart method (7) (CO1)

P.T.O

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Foster socially responsible technocrats and entrepreneurs who contribute positively to society through their expertise and leadership.

Present State	Next State x=0	Next State x=1	Output x=0	Output x=1
a	d	b	0	0
b	e	a	0	0
c	g	f	0	1
d	a	d	1	0
e	a	d	1	0
f	c	b	0	0
g	a	e	1	0

b. Implement ASM chart for a Binary up down counter with suitable sketches (7) (CO1)

6. a. Analyse the clocked synchronous sequential circuit. The excitation input and output equations are given. D1 = x'Q2' + Q1'Q2 , D2 = xQ1'+Q1'Q2 , Z = x'Q1+ xQ1'Q2' . Construct the excitation table and transition table (7) (CO2)

b. Draw the State table and state diagram for the above problem (7) (CO2)

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