Name:.....
Roll No:.....

MAR ATHANASIUS COLLEGE OF ENGINEERING (AUTONOMOUS),
KOTHAMANGALAM - 686666
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

B.TECH FIRST SERIES EXAMINATION, AUGUST 2026 (S3 CS, DS, AIML)
B24CS2T02 COMPUTER ORGANIZATION AND ARCHITECTURE

Max. Marks: 40 Duration: 1.5 Hours

PART A

Answer all questions. Each question carries 3 marks.

1. A 32-bit machine stores ASCII characters from the keyboard in successive byte addresses starting at 4000H. Determine the memory content for the string 'ALICE' in both endian formats. (A=41, L=4C, I=49, C=43, E=45, unused=xx) **(CO1)**

2. i) SUB R1, R2
   ii) MOV R3, #100
   iii) MOV -(SP), R4

   Identify the addressing mode used in each instruction.

   (CO1)

3. Two processors each have the same total memory capacity of 1 MB. Processor A is word-addressable with a word size of 2 bytes, while Processor B is byte-addressable. For both processors, determine:
   i) The number of distinct addressable locations.
   ii) The minimum number of address lines required for each.

   (CO2)

4. Define bias in floating-point representation. Why is it used? **(CO2)**

PART B

Answer all questions. Each question carries 14 marks.

5. Consider the instruction ADD R1, (R3), where R1 $\leftarrow$ R1 + Mem(R3). Draw the single-bus and multi-bus datapath organizations, and specify the sequence of control signals required to execute the instruction in each organization.

   (CO1)(14 marks)

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6. (a) Explain data hazards with examples of RAW (Read After Write), WAR (Write After Read), and WAW (Write After Write) hazards. **(CO2)**(6 marks)

(b) Consider the following instruction sequence executed on a five-stage instruction pipeline consisting of the stages Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB), where all stages have equal execution time. Identify and classify the pipeline hazards present in the instruction sequence. Explain how each hazard can be resolved, and discuss the appropriate techniques that can eliminate or minimize the pipeline stalls caused by these hazards.

I1: LOAD R4, [R5], Contents of mem [R5] is loaded to R4
I2: ADD , R4, R7, R4←R7+R4
I3: STORE [R8],R6 Contents of R6 is stored to mem[R8]
I4: SUB R5, R6, R5←R5-R6
I5: JMP 1000, jump to LOC[1000]
I6: MOV R7, R8, R7←R8

(CO2)(8 marks)

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