

Reg No.: _____

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (S,FE) (FT/WP) / S1 (PT) Examination November/December 2025 (2019 Scheme)

Course Code: ECT203**Course Name: LOGIC CIRCUIT DESIGN**

Max. Marks: 100

Duration: 3 Hours

PART A*Answer all questions. Each question carries 3 marks*

Marks

- 1 Perform the following Conversions (3)
 - (i) Binary number 10011101 to gray code
 - (ii) Binary number 10110011 to Octal
 - (iii) BCD number 10011100 to Excess-3 code
- 2 With the help of an example, differentiate the working of following Verilog HDL keywords. (a) Monitor (b) display (3)
- 3 State De-Morgan's theorem and obtain the complement of the function (3)
 $F_1 = X'YZ + XY'Z'$ using De-Morgan's theorem.
- 4 Obtain the truth table of the following function. (3)
 $F = (A+B)(A'+B+C)(A+B'+C)$
- 5 A test bench is designed to test a Verilog description of a full subtractor with X, Y, Z as its inputs and D&B as its outputs. Draw the timing diagram that will be produced by the simulator for the following stimulus. (3)
initial begin
 X = 0; Y = 0; Z = 1;
#2 X = 0; Y = 1; Z = 0;
#4 X = 0; Y = 1; Z = 1;
#3
end
- 6 Construct a 2-bit full subtractor using half subtractors. Use minimum hardware. (3)
- 7 What is excitation table of a flip flop? Give the excitation table of SR flip flop. (3)
- 8 Show the construction of JK flip-flop from D-flip-flop. (3)
- 9 Draw the circuit of a CMOS inverter and identify the components and terminals. (3)
- 10 Explain the terms "setup time" & "hold time" of a digital integrated circuit. (3)

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PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

- 11 a. Generate Hamming code with odd parity for the 8-bit data word "11010101". (8)
- b. With the help of suitable examples, explain the data types used in Verilog HDL. (6)
- 12 a. Given the two octal numbers $A = (56)_8$ and $B = (160)_8$. Obtain $(Y)_8 = A - B$ using 1's complement & 2's complement. (8)
- b. Explain the following codes with suitable examples. (6)
- i BCD code ii Excess 3 code iii Parity check codes
 - iv ASCII Code

Module 2

- 13 a. Draw the logic diagram of a 2-input XOR gate using NOR gate and implement it using Verilog code. Use gate-level modeling. (8)
- b. Convert each of the following into the other canonical form: (6)
- i. $F(x, y, z) = \sum m(1, 2, 4, 5)$
 - ii. $F(A, B, C, D) = \prod M(3, 5, 8, 10)$
 - iii. $F(p, q, r, s) = \sum m(0, 3, 7, 10, 12)$
 - iv. $F(A, B, C) = \prod M(0, 1, 4, 6,)$
- 14 a. Draw the logic diagram corresponding to the following Boolean expressions without simplifying them. (10)
- i. $(A + C)(C + D')(A' + B + D)$
 - ii. $(AC + A'B')(BD' + C'D)$
 - iii. $A + CD + (A + D')(C' + D)$
 - iv. $AB' + AD + AC'D$
- b. Obtain the simplified Boolean expression from the following Boolean function using K-map (4)

$$F(a, b, c) = \sum m(1, 3, 4, 6)$$

Module 3

- 15 a. Design a 1-bit comparator, which tests only the following condition $Y = A \geq B$, where A & B are one-bit inputs and Y is one-bit output. (8)
- b. Construct a 4-bit BCD adder using 4-bit parallel adders and logic gates. (6)

(Mark the inputs and outputs properly.)

- 16 a. Implement the following logic function using 8:1 and 4:1 multiplexers. (8)

$$G(a, b, c) = \sum m(0, 3, 5, 6)$$

- b. Write a Verilog code for implementing a 4-bit binary to Gray-code encoder. (6)

Module 4

- 17 Using positive edge triggering JK flip flops, design a synchronous counter (14)
which counts in the following sequence: 000, 111, 110, 101, 100, 011, 010, 001, 000.....

- 18 a. Design a Mod-9 asynchronous counter using JK flip flops. (9)
b. Derive the characteristic equation of SR flip flop (5)

Module 5

- 19 a. With the help of a circuit diagram, explain the working of a CMOS (8)
NAND gate.
b. Compare the Characteristics of TTL & CMOS digital logic families. (6)
- 20 a. Explain the working of TTL inverter with the help of a circuit diagram. (8)
b. Following are the specifications of a TTL gate: $V_{CC}=5V$, $I_{CCH}=20mA$, $I_{CCL}=40mA$, $t_{PHL}=3ns$, $t_{PLH}=3ns$, $V_{OH}=2.7V$, $V_{OL}=0.5V$, $V_{IH}=2V$, $V_{IL}=0.8V$. Calculate the average propagation delay and noise margin of the TTL gate. (6)
