QP Code:EC2T07-1 **(Pages:2)**

Reg No : ..... Name : .....

MAR ATHANASIUS COLLEGE OF ENGINEERING, KOTHAMANGALAM

(Govt. Aided Autonomous Institution)

Fourth Semester B.Tech. Degree Examination, May, 2026

Course Code: B24EC2T07

Course Name: FPGA BASED SYSTEM DESIGN

Max. Marks: 100 Duration:3 Hours

PART - A: 30 Marks (10 Qns x 3 Marks)

Answer all questions

1. Write a Verilog gate-level module for a 1-bit greater-than circuit.
2. Write a gate-level Verilog statement for a 2-input AND gate.
3. Explain the significance of the sensitivity list in an always block.
4. Write the general syntax of an if–else statement in Verilog.
5. Design a 5-bit free running shift register using Verilog HDL with a clock and reset input, a 1-bit serial input (d_in), and a 1-bit serial output (d_out). The register shall shift data to the right on every clock edge.
6. Sketch the block diagram of a synchronous sequential system.
7. What is state transition? Explain with a simple example of a 2-state FSM.
8. Draw the state diagram of a Mealy finite state machine for a rising edge detector.
9. Define an ASMD chart and state its purpose in digital design.
10. What is the function of the decrement counter used in the debouncing circuit? Write a verilog code for a decrement counter that generates a tick signal every 1 msec, given clock frequency is 50MHz.

PART - B: 70 Marks (5 Qns x 14 Marks)

Answer any One full question from each module.

Module 1

11. (a) How number representation can be done in Verilog with suitable examples? (7 marks)

    (b) Write a Verilog gate-level code for a 2-to-4 binary decoder and explain its operation. (7 marks)

OR

12. Discuss about logic cells in FPGA and explain FPGA design flow.

Module 2

13. (a) Write a Verilog module using arithmetic and relational operators to compare two numbers and generate an output. (7 marks)

(b) Write a Verilog code to find the largest of two numbers using operators. (7 marks)

OR

14. (a) Explain the concept of number representation in Verilog HDL with examples. (7 marks)

(b) Write and explain a Verilog code for a digital 4 to 2 encoder. (7 marks)

Module 3

15. Design a 12 bit up/down counter using Verilog HDL with enable, direction input (up/down) and both synchronous and asynchronous reset signals.

OR

16. Explain how a programmable square-wave generator can produce different output frequencies from a single clock source. Design a programmable square-wave generator using a counter and write the Verilog HDL code to generate multiple selectable frequencies.

Module 4

17. Write a Verilog HDL program to design a circuit that detects a push-button input using debouncing and timing logic such that a short press increments a counter by 1 and a long press resets the counter to zero.

OR

18. Develop verilog code for moore 1010 sequence detector.

Module 5

19. Explain the complete procedure for developing Verilog code for an FSMD starting from an ASMD chart. Give example?

OR

20. Design a system using Verilog HDL to accurately measure a low-frequency input signal using a high-frequency clock. Develop the FSMD structure and write the code.

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