**QP Code:EC1T03-3** **(Pages: 2)**

Reg No : ..... Name : .....

**MAR ATHANASIUS COLLEGE OF ENGINEERING, KOTHAMANGALAM**

(Govt. Aided Autonomous Institution)

Second Semester B.Tech. Degree Examination, May, 2026

Course Code: B24EC1T03

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 100 Duration:3 Hours

**PART - A: 30 Marks (10 Qns x 3 Marks)**

**Answer all questions**

1. Find gray code of decimal number 15?
2. Convert the decimal number (0.356) to its hexadecimal equivalent.
3. Find the complement of the functions F1=x'. y. z'+x'. y'. z and F2= x(y'. z'+y. z).
4. Simplify the Boolean function x(x' + y) to a minimum number of literals.
5. Explain the working of a 1-bit comparator with its truth table and logic equations.
6. Explain the working of 4-bit Binary Parallel Adder. How does the carry-in bit contribute to its operation?
7. Differentiate asynchronous and synchronous counters with examples.
8. How does a Johnson counter differ from a Ring counter? Write a 3-bit Johnson sequence.
9. Explain the role of the totem-pole output stage in a TTL inverter.
10. Explain transition time with an example.

**PART - B: 70 Marks (5 Qns x 14 Marks)**

**Answer any One full question from each module.**

**Module 1**

11. Consider the signed binary numbers A = 01000110 and B = 11010011 where B is in 2's complement form. Find the value of the following mathematical expression.

a) (-A) + (-B) (3 marks)

b) A - B (3 marks)

c) B-A (3 marks)

d) -A-B (3 marks)

(e) A+B (2 marks)

OR

12. A digital system uses binary arithmetic for its computations. Solve the following binary operations step by step, showing all calculations:

a) Perform the binary addition of $1011011_2$ and $1101101_2$ (4 marks)

b) Perform the binary subtraction $1101011_2 - 1010110_2$ using the borrow method (4 marks)

c) Multiply $1011_2$ by $110_2$ using the long multiplication method (3 marks)

d) Divide $101101_2$ by $11_2$ using binary division (3 marks)

**Module 2**

13. Minimize $F(A, B, C, D) = \pi( 2, 3, 8,12, 13).d(10,14)$ using Tabulation Method.

OR

14. Simplify using K-map

a) $F(A, B, C, D) = \Sigma(0, 1, 2, 5, 6, 8, 9, 10, 14)$ (6 marks)

b) $F(A, B, C, D,E) = \Sigma(0, 1,6,7,8,9,21,22,23,29,31)$ (8 marks)

**Module 3**

15. a) Explain a 3:8 Decoder with a logic diagram. (7 marks)

b) Explain the working of a BCD to Excess-3 Code Converter. (7 marks)

OR

16. a) Design a Full Adder using two Half Adders and an OR gate. (7 marks)

b) Implement Half Adder circuit using universal NOR gate. (7 marks)

**Module 4**

17. a) What is an Up-Down counter? Explain its working with a circuit diagram and truth table. (6 marks)

b) Design a BCD counter using JK Flip-Flops. Explain its working with a state diagram and truth table. List out its applications. (8 marks)

OR

18. a) Explain the working of a Master-Slave JK Flip-Flop. (7 marks)

b) Convert a JK Flip-Flop into a D Flip-Flop. (7 marks)

**Module 5**

19. a) Describe the working of a tristate TTL inverter. (8 marks)

b) Explain the working of a transistor level CMOS NAND gate. (6 marks)

OR

20. State and explain the advantageous of CMOS logic families when compared to the other logic families. Also draw and explain the structure and working of a 2 input CMOS NAND gate.

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