

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (S,FE) (FT/WP) / S1 (PT) Examination November/December 2025 (2019 Scheme)

Course Code: CST203**Course Name: Logic System Design**

Max. Marks: 100

Duration: 3 Hours

PART A*Answer all questions. Each question carries 3 marks*

Marks

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| 1 | Subtract the following decimal numbers by the 9's complement method.
i) $574.6 - 279.7$ ii) $435 - 645$ | (3) |
| 2 | What are error detecting codes? How we detect errors in codes? | (3) |
| 3 | Find complement of the given functions.
i) $ABEF + ABE'F' + A'B'EF$ ii) $AB' + BC' + AC$ iii) $A' \cdot (B+C') + (A'B'C)$ | (3) |
| 4 | Express the following function as sum of min terms and product of max terms:
i) $F(A,B,C) = A' + B + CA$ ii) $F(A,B,C) = B(A' + B' + C')(A + B')$ | (3) |
| 5 | Implement the logic function $A \odot B$, using 4x1 MUX. | (3) |
| 6 | Derive the simplified Boolean output functions of a full subtractor. | (3) |
| 7 | Differentiate between edge triggered and level triggered flip flops. | (3) |
| 8 | Give the excitation table of T flip flop. | (3) |
| 9 | Explain the working of serial in parallel out shift register. | (3) |
| 10 | Write short notes on PLA. | (3) |

PART B*Answer any one full question from each module. Each question carries 14 marks***Module 1**

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| 11.(a) | Perform the following conversions using suitable steps.
i) $(61.3125)_{10}$ to binary ii) $(242.257)_8$ to hexadecimal
iii) $(110101.101010)_2$ to octal iv) $(4A01)_{16}$ to binary | (8) |
| (b) | Describe the different schemes for representing negative numbers with proper examples. | (6) |
| 12.(a) | Convert the decimal numbers 534 and 281 into BCD and do the addition and subtraction operation in BCD arithmetic. | (8) |
| (b) | Perform the following arithmetic operations:
i) $(164.57)_8 + (537.1)_8$ ii) $(F9AC)_{16} - (D4C7)_{16}$
iii) $46 - 14$ using 2's complement method. | (6) |

Module 2

- 13.(a) Simplify the Boolean function $F(A, B, C, D) = \sum m(1,3,5,8,9,11,15) + d(2,13)$ using Quine-McCluskey method. (10)
- (b) Implement the given function $F = (A+B').C.(B+C)$ (4)
i) using OR, AND logic gates ii) using only NOR gates
- 14.(a) Minimise the following functions by K-map method and realize using minimum number of gates (10)
i) $F1 = \sum m(0,1,2,3,11,12,14,15)$ ii) $F2 = \pi M(1,4,6,9,10,11,14,15)$.
- (b) Reduce the following Boolean expression to minimum number of literals (4)
i) $AB + (AC)' + AB'C(AB+C)$ ii) $((X'Y' + Z))' + Z + XY + WZ$

Module 3

- 15.a) Design and implement a 2-bit magnitude comparator using 4 X 16 decoder. (7)
- (b) With the help of a logic diagram explain 3-bit BCD to binary code converter. (7)
- 16.(a) How can the principle of look-ahead carry reduce the carry propagation time in a binary parallel adder? Derive the Boolean functions for the carry outputs at different stages of a look-ahead carry generator. (9)
- (b) Design and implement full adder by using only NAND gates. (5)

Module 4

- 17.(a) Explain race around condition in JK flip-flop. Explain how a master slave flip flop avoids race around condition. (7)
- (b) Design a counter that goes through states 0, 3,5,6,0 (7)
- 18.(a) What is a BCD ripple counter? Explain its operation by means of logic and timing diagram. (9)
- (b) How a D-flip flop can be converted to J-K flip-flop? (5)

Module 5

- 19.(a) Give the IEEE Single precision format for floating point number representation with explanation. Determine the floating-point binary number represented by the following single precision floating point representation. "0100 0011 0101 0100 0000 0000 0000 0000" (8)
- (b) Implement a 4-bit bidirectional shift register with parallel load. (6)
- 20.(a) Draw a flow chart and explain the addition/ subtraction of signed 2's complement representation. (7)
- (b) Explain the working of 4-bit Johnson counter with a timing diagram. (7)
