QP CodeA:CS1T01-2 **(Pages: 3)**

Reg No : ..... Name : .....

MAR ATHANASIUS COLLEGE OF ENGINEERING, KOTHAMANGALAM

(Govt. Aided Autonomous Institution)

Second Semester B.Tech. Degree Examination, May, 2026

Course Code: B24CS1T01

Course Name: LOGIC SYSTEM DESIGN

Max. Marks: 100 Duration:3 Hours

PART - A: 30 Marks (10 Qns x 3 Marks)

Answer all questions

1. State and explain De Morgan's law.
2. Define the terms i) Prime Implicants ii) Essential Prime Implicants. iii) Non-Essential Prime Implicants.
3. Design a half adder circuit from its truth table.
4. Define the terms 'Generate' (G) and 'Propagate' (P) in a Carry Look-Ahead Adder.(3 marks)
5. What is an excitation table and how is it useful in flip-flop?
6. Explain the role of the load signal in a parallel load register.
7. Explain the operation of a 2-bit Johnson counter.
8. List any three data types in Verilog with an example for each.
9. Describe the process of converting a decimal number to a fraction and perform the conversion with an example.
10. Write the steps to find the 2's complement of a binary number.

PART - B: 70 Marks (5 Qns x 14 Marks)

Answer any One full question from each module.

Module 1

11. a) Simplify the Boolean function F(a,b,c,d) = ∑m (0,1,2,5,7,8,9,10,11,13,15) using K map (7 marks)

    b) Find the reduced POS using K Map F(a,b,c,d)= ΠM(3,6,8,11,13,14) **.** d(1,5,7,10) (7 marks)

OR

12. a) Expand F(A,B,C) = $A + B\bar{C} + AB\bar{D} + ABCD$ to minterms and maxterms. (7 marks)

b) Express the logical function F (A,B,C,D) = $\bar{B}D + \bar{A}D + BD$ as sum of minterms and product of maxterms. (7 marks)

Module 2

13. a) Design a code converter circuit for converting Excess -3 to BCD number. (8 marks)

b) In an even parity scheme, which of the following words contains an error?

(i) 10101010 (ii) 11110110 (iii) 10111001 (6 marks)

OR

14. In a keyboard interface system, an encoder is used to convert key presses into binary codes that are sent to the computer. (a) Explain how the encoder assigns unique binary codes to different keys when multiple keys are pressed simultaneously. (b) Draw the truth table showing the binary output for at least 8 different keys. (c) Discuss one potential issue that may arise if two keys are pressed at the same time and suggest a solution to handle this scenario effectively.

Module 3

15. Design a 5 bit asynchronous up/ down counter using J K Flip Flop.

OR

16. a) Design a BCD counter using T flipflop. (9 marks)

b) Design a type D counter that goes through states 0,3,5,6,0..... (5 marks)

Module 4

17. Explain how sensitivity lists are used in Verilog when modeling D flip-flops. Discuss their impact on simulation behavior.

OR

18. Explain the Parallel-In Parallel-Out (PIPO) shift register and describe its role in temporary data storage.

Module 5

19. Illustrate the algorithm for addition and subtraction of two BCD numbers with suitable examples.

OR

20. Explain the binary division process using the restoring method with an example. Include all intermediate steps and calculations.

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